IN THE CLAIMS:

1.-9. **(Canceled)**

10. **(Currently Amended)** A method for hiding devices from a computer host, said devices and host sharing a common electrical bus, said method comprising:

providing one or more expansion slots configured to receive a respective add-in card including a processor therein;

generating a signal indicative of the presence of said add-in card in one of the expansion slots;

in response to said signal indicative of the presence of said add-in card, non-intermittently masking a host device select signal generally used by said host to assert control of a controller on the motherboard of said host; ~~and~~

~~propagating~~imparting a predefined time delay to a bus grant signal configured to grant control rights to the processor on said add-in card, in lieu of said host, over said controller, wherein said time delay corresponds to a clocking cycle of a clocking signal for said electrical bus; and

propagating said bus grant signal to said controller upon completion of said clocking cycle and the signal indicative of the presence of said add-in card actually indicating the presence of said add-in card in one of the expansion slots, thereby propagating said bus grant signal synchronously with the clocking signal for said electrical bus for effecting the control rights of said processor over said controller.

11. **(Original)** The method for hiding devices of claim 10 wherein said electrical bus comprises a peripheral connect interface bus.

12. **(Currently Amended)** The method for hiding devices of claim 11 wherein said ~~the~~ processor on said add-in card comprises a RAID processor.

13. **(Original)** The method for hiding devices of claim 12 wherein said controller on the motherboard of the host comprises an I/O controller.

14. **(Currently Amended)** The method for hiding devices of claim 10 further comprising passing the host device select signal from the host to the ~~second peer device~~controller in the absence of said ~~first peer device~~add-in card.

15. **(Currently Amended)** A circuit for hiding peer devices from a computer host, said devices and host sharing a common electrical bus generally controlled by said host, said circuit comprising:

a generating module configured to supply a signal indicative of the presence of a first peer device; ~~and~~

a hiding module configured to non-intermittently hide a second peer device from said host so that said second device is controlled by said first peer device whenever said signal indicates the presence of said first peer device, wherein said hiding module comprises a masking module coupled to receive said signal indicative of the presence of said first device to mask a host device select signal generally supplied by the host to said second peer device; and

a delay device for imparting a predefined time delay to a bus grant signal configured to grant control rights to the first peer device, in lieu of said host, over said second peer device, wherein said time delay corresponds to a clocking cycle of a clocking signal for said electrical bus, said delay device electrically coupled to propagate said bus grant signal to said second peer device upon completion of said clocking cycle and the signal indicative of the presence of the first peer device actually indicating the presence of said first device, thereby propagating said bus grant signal synchronously with the clocking signal for said electrical bus for effecting the control rights of said first peer device over said second peer device.

16. **(Canceled)**

17. **(Original)** The circuit for hiding peer devices of claim 15 wherein said electrical bus comprises a peripheral connect interface bus.

18. **(Original)** The circuit for hiding peer devices of claim 17 wherein said first peer device comprises a RAID processor.

19. **(Original)** The circuit for hiding peer devices of claim 18 wherein said second peer device comprises an I/O controller.

20. **(Original)** The circuit for hiding peer devices of claim 19 wherein said I/O controller is embedded in a motherboard of the host.

21. **(Original)** The circuit for hiding peer devices of claim 20 wherein said RAID processor is disposed on an add-in card.

22. **(Original)** The circuit for hiding peer devices of claim 15 wherein said masking module is further configured to pass the host select signal from the host to the second peer device in the absence of said first peer device.

23. **(Currently Amended)** The circuit of claim 16 wherein said ~~propagating module~~delay device comprises a flip-flop.

24. **(Original)** The circuit of claim 16 wherein said masking module comprises a plurality of switches.

25. **(Original)** The circuit of claim 16 wherein said masking module comprises a plurality of logical gates.